# INTRODUCTION TO DIGITAL SIGNAL PROCESSORS (DSPs)


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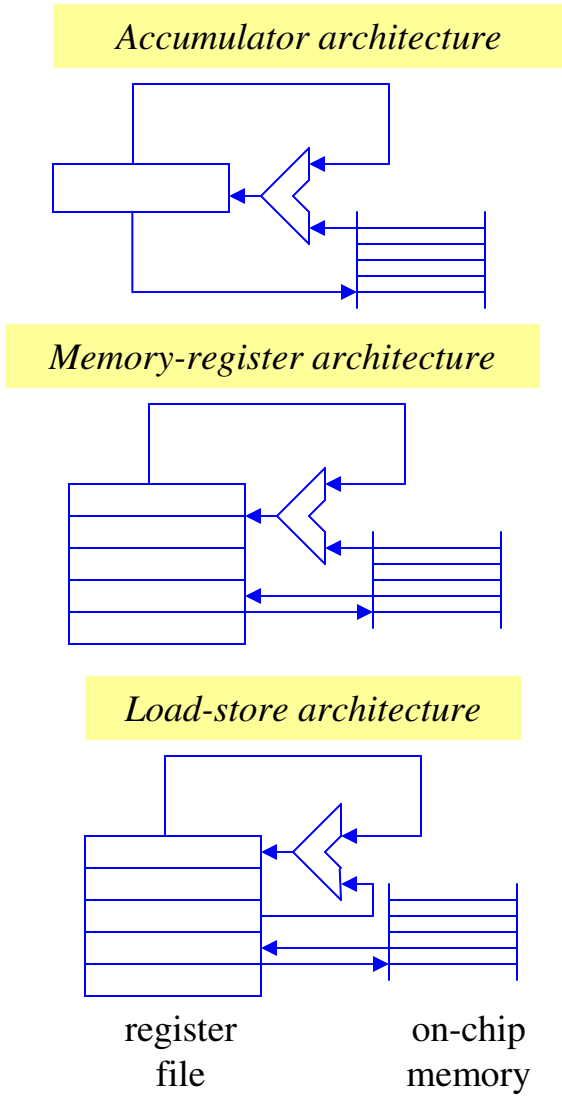


# Outline

- Signal processing applications
- Conventional DSP architecture
- Pipelining in DSP processors
- RISC vs. DSP processor architectures
- TI TMS320C6000 DSP architecture introduction
- Signal processing on general-purpose processors
- Conclusion

# Signal Processing Applications

- Embedded system demand in world: volume, volume, …
  - *400 Million units/year:* automobiles, PCs, cell phones
  - *30 Million units/year:* ADSL modems and printers
- Consumer electronics products

| Product | Average Unit Price | Annual Revenue |
|---|---|---|
| Wireless phone | $136 | $11.5 Billion |
| Digital cameras | $271 | $ 4.2 Billion |
| Portable CD players | $ 48 | $ 0.9 Billion |
| MP3 players | $137 | $ 0.7 Billion |
| Compact audio systems | $111 | $ 0.5 Billion |

Source: CEA Market Reseach (US). Data for 2004 calendar year.

- How much should an embedded processor cost?

# Signal Processing Applications

- Embedded system cost and input/output rates
  - *Low-cost, low-throughput:* sound cards, cell phones, MP3 players, car audio, guitar effects
  - *Medium-cost, medium-throughput:* low-end printers, disk drives, PDAs, ADSL modems, digital cameras, video conferencing
  - *High-cost, high-throughput:* high-end printers, audio mixing boards, wireless basestations, high-end video conferencing, 3-D sonar, 3-D reconstructions from 2-D slices (e.g. X-rays) in medical imaging
- Embedded processor requirements
  - Inexpensive with small area and volume
  - Predictable input/output (I/O) rates to/from processor
  - Power constraints (severe for handheld devices)

**Single DSP**

**Single DSP + Coprocessor**

**Multiple DSPs**

# Conventional DSP Processors

- Low cost: as low as $2/processor in volume
- Deterministic interrupt service routine latency guarantees predictable input/output rates
  - On-chip direct memory access (DMA) controllers
    - Processes streaming input/output separately from CPU
    - Sends interrupt to CPU when block has been read/written
  - Ping-pong buffering
    - CPU reads/writes buffer 1 as DMA reads/writes buffer 2
    - After DMA finishes buffer 2, roles of buffers 1 & 2 switch
- Low power consumption: 10-100 mW
  - TI TMS320C54 0.32 mA/MIP → 76.8 mW at 1.5 V, 160 MHz
  - TI TMS320C55 0.05 mA/MIP → 22.5 mW at 1.5 V, 300 MHz
- Based on conventional (pre-1996) architecture

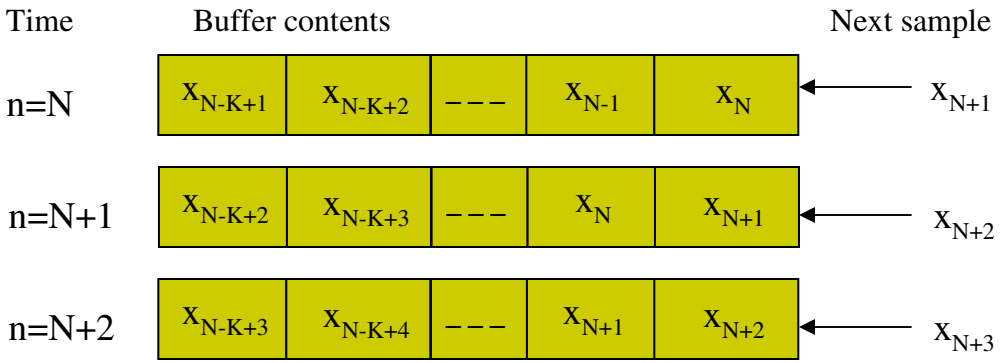
# Conventional DSP Architecture

- Multiply-accumulate (MAC) in 1 instruction cycle
- Harvard architecture for fast on-chip I/O
  - Data memory/bus separate from program memory/bus
  - One read from program memory per instruction cycle
  - Two reads/writes from/to data memory per inst. cycle
- Instructions to keep pipeline (3-6 stages) full
  - Zero-overhead looping (one pipeline flush to set up)
  - Delayed branches
- Special addressing modes supported in hardware
  - Bit-reversed addressing (e.g. fast Fourier transforms)
  - Modulo addressing for circular buffers (e.g. filters)

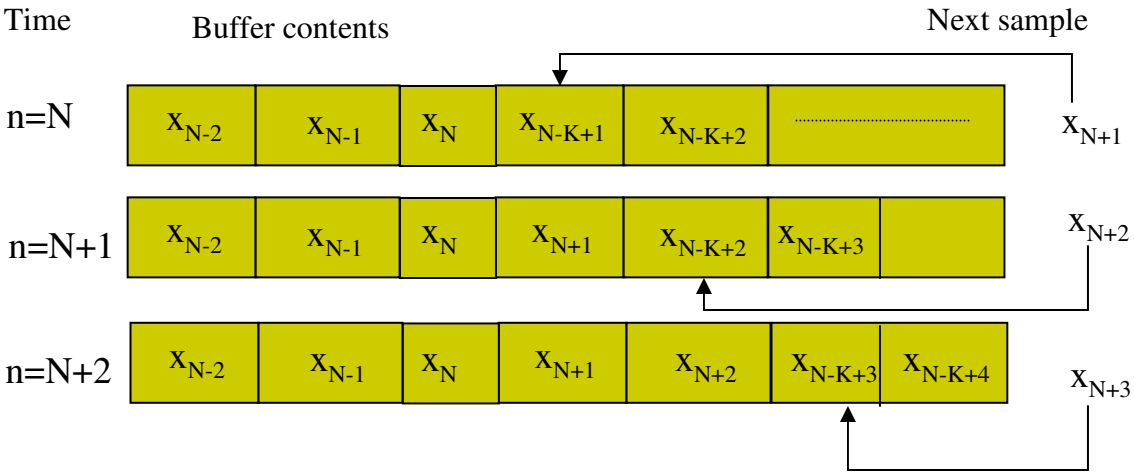
# Conventional DSP Architecture (con't)

- Buffer of length *K*
  - Used in finite and infinite impulse response filters
- Linear buffer
  - Sort by time index
  - Update: discard oldest data, copy old data left, insert new data
- Circular buffer
  - Oldest data index
  - Update: insert new data at oldest index, update oldest index

**Data Shifting Using a Linear Buffer**




**Modulo Addressing Using a Circular Buffer**



# Conventional DSP Processors Summary

| | *Fixed-Point* | *Floating-Point* |
|---|---|---|
| ***Cost/Unit*** | $2 - $79 | $3 - $381 |
| ***Architecture*** | Accumulator | load-store or memory-register |
| ***Registers*** | 2-4 data<br>8 address | 8 or 16 data<br>8 or 16 address |
| ***Data Words*** | 16 or 24 bit integer and fixed-point | 32 bit integer and fixed/floating-point |
| ***On-Chip Memory*** | 2-64 kwords data<br>2-64 kwords program | 8-64 kwords data<br>8-64 kwords program |
| ***Address Space*** | 16-128 kw data<br>16-64 kw program | 16 Mw – 4Gw data<br>16 Mw – 4 Gw program |
| ***Compilers*** | C, C++ compilers; poor code generation | C, C++ compilers; better code generation |
| ***Examples*** | TI TMS320C5000; Freescale DSP56000 | TI TMS320C30; Analog Devices SHARC |

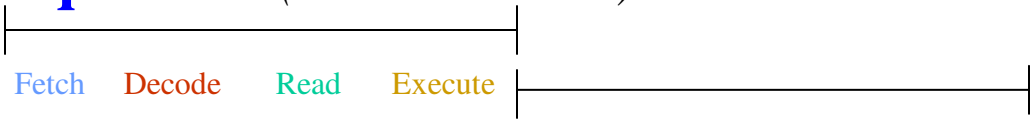
# Conventional DSP Processor Families

**DSP Market (est.)**
**Fixed-point 95%**
**Floating-point 5%**

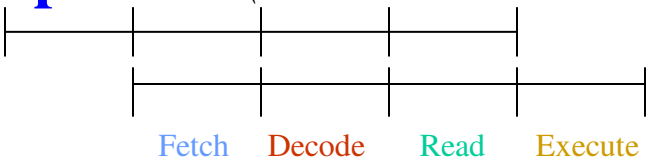
- Floating-point DSPs
  - Used in initial prototyping of algorithms
  - Resurgence due to professional and car audio
- Different on-chip configurations in each family
  - Size and map of data and program memory
  - A/D, input/output buffers, interfaces, timers, and D/A
- Drawbacks to conventional DSP processors
  - No byte addressing (needed for images and video)
  - Limited on-chip memory
  - Limited addressable memory on fixed-point DSPs (exceptions include Freescale 56300 and TI C5409)
  - Non-standard C extensions for fixed-point data type

# Pipelining

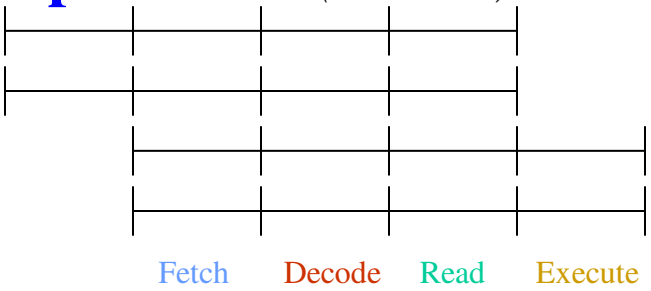
**Sequential** *(Freescale 56000)*



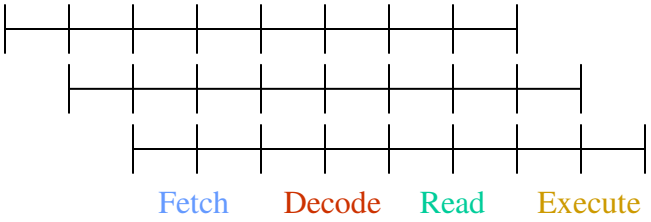

**Pipelined** *(Most conventional DSPs)*




**Superscalar** *(Pentium)*




**Superpipelined** *(TMS320C6000)*




## *Pipelining*

- Process instruction stream in stages (as stages of assembly on a manufacturing line)
- Increase throughput

## *Managing Pipelines*

- Compiler or programmer
- Pipeline interlocking

# Pipelining: Operation

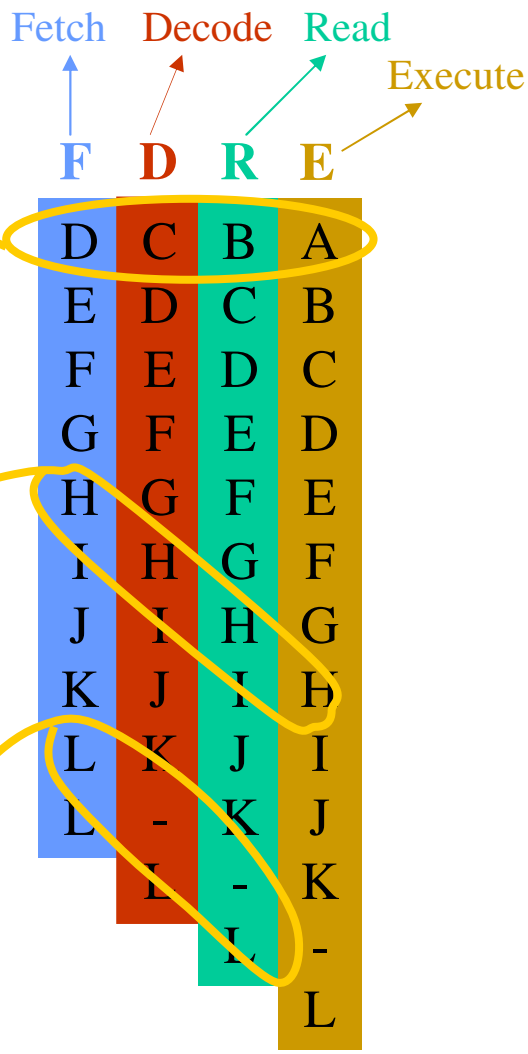
- Time-stationary pipeline model
  - Programmer controls each cycle
  - Example: Freescale DSP56001 (has separate X/Y data memories/registers)

```
MAC X0,Y0,A  X:(R0)+,X0 Y:(R4)-,Y0
```

- Data-stationary pipeline model
  - Programmer specifies data operations
  - Example: TI TMS320C30

```
MPYF *++AR0(1),*++AR1(IR0),R0
```

- Interlocked pipeline
  - "Protection" from pipeline effects
  - May not be reported by simulators: inner loops may take extra cycles



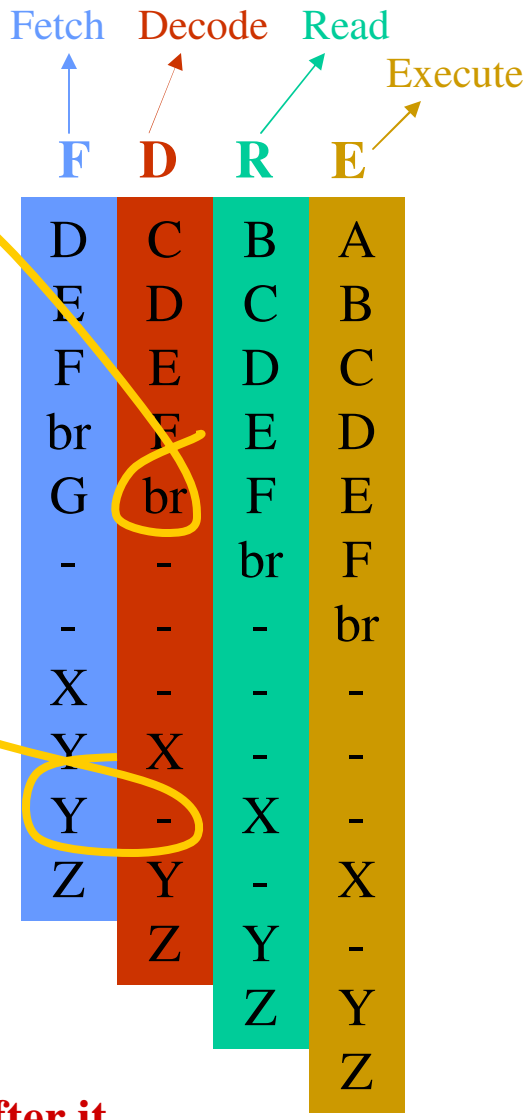

*MAC means multiplication-accumulation.*

# Pipelining: Hazards

- A control hazard occurs when a branch instruction is decoded
  - Processor "flushes" the pipeline, or
  - Use delayed branch (expose pipeline)
- A data hazard occurs because an operand cannot be read yet
  - Intended by programmer, or
  - Interlock hardware inserts "bubble"
  - TI TMS320C5000 (20 CPU & 16 I/O registers, one accumulator, and one address pointer ARP implied by *)

```
LAR  AR2, ADDR ; load address reg.
LACC *-        ; load accumulator w/
               ; contents of AR2
```

**LAR: 2 cycles to update AR2 & ARP; need NOP after it**

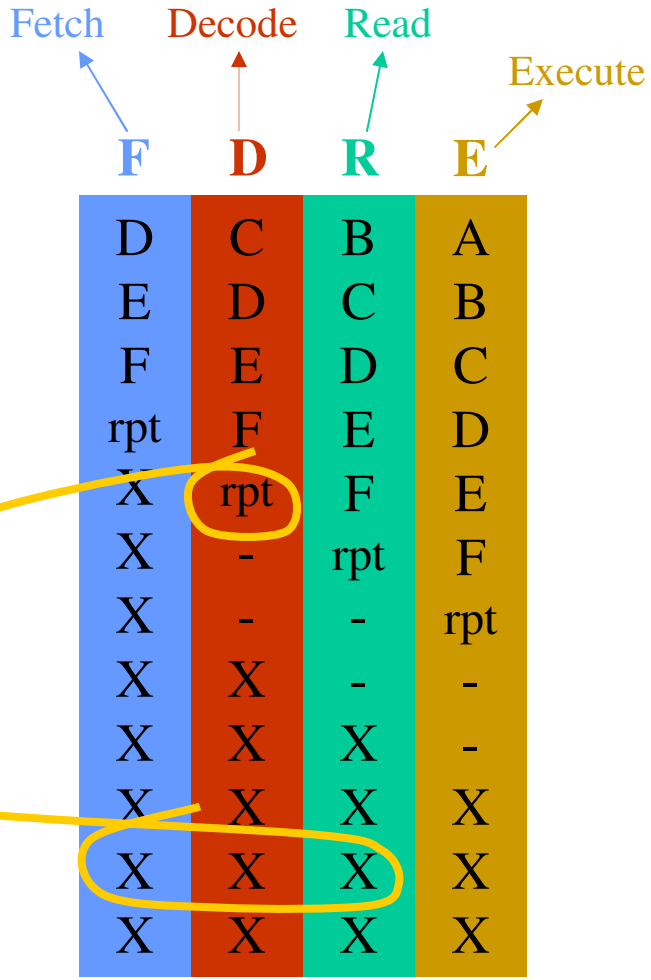


# Pipelining: Avoiding Control Hazards

High throughput performance of DSPs is helped by on-chip dedicated logic for looping (downcounters/looping registers)

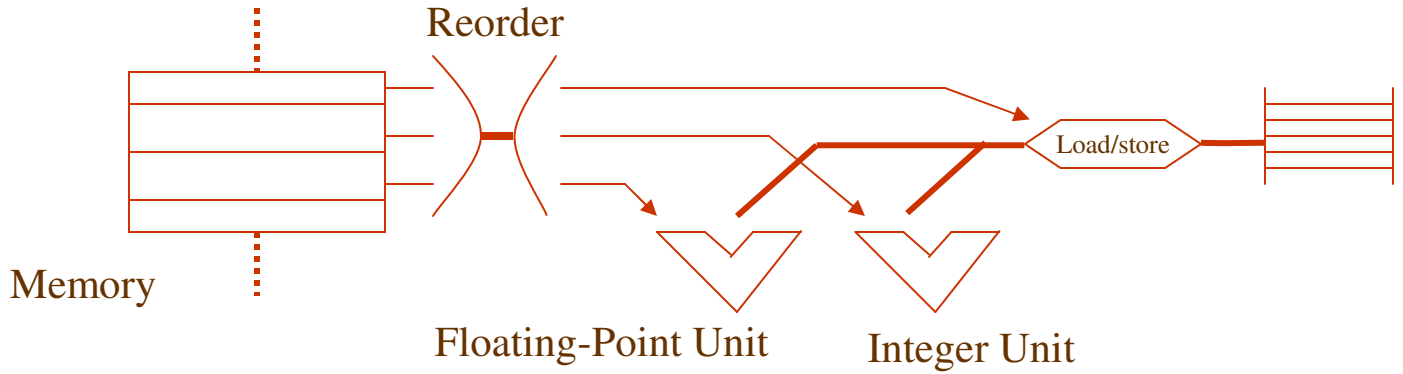
```
; repeat TBLR inst. COUNT-1 times
RPT COUNT
TBLR *+
```

- A repeat instruction repeats one instruction or a block of instructions after repeat
- The pipeline is filled with repeated instruction (or block of instructions)
- Cost: one pipeline flush only

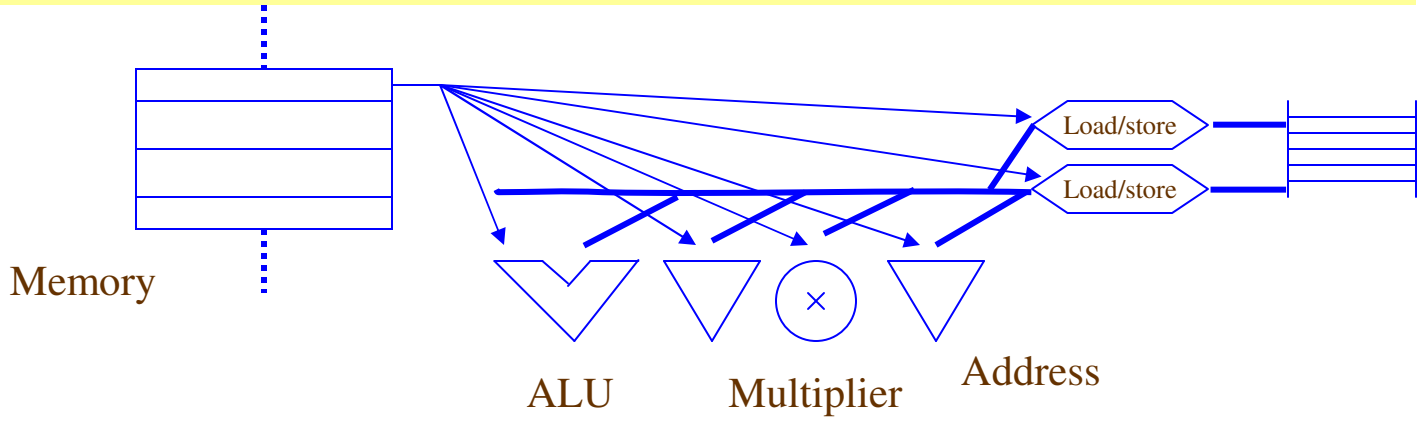


# RISC vs. DSP: Instruction Encoding

- RISC: Superscalar, out-of-order execution

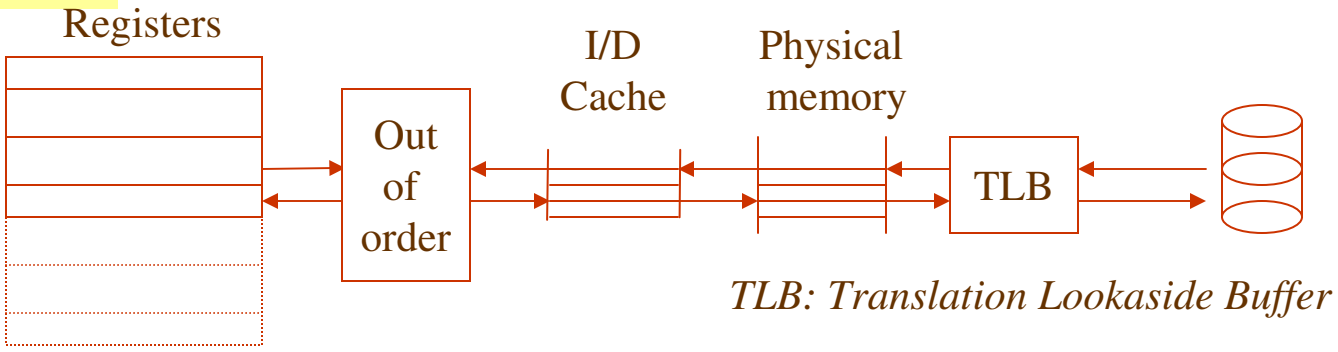



- DSP: Horizontal microcode, in-order execution



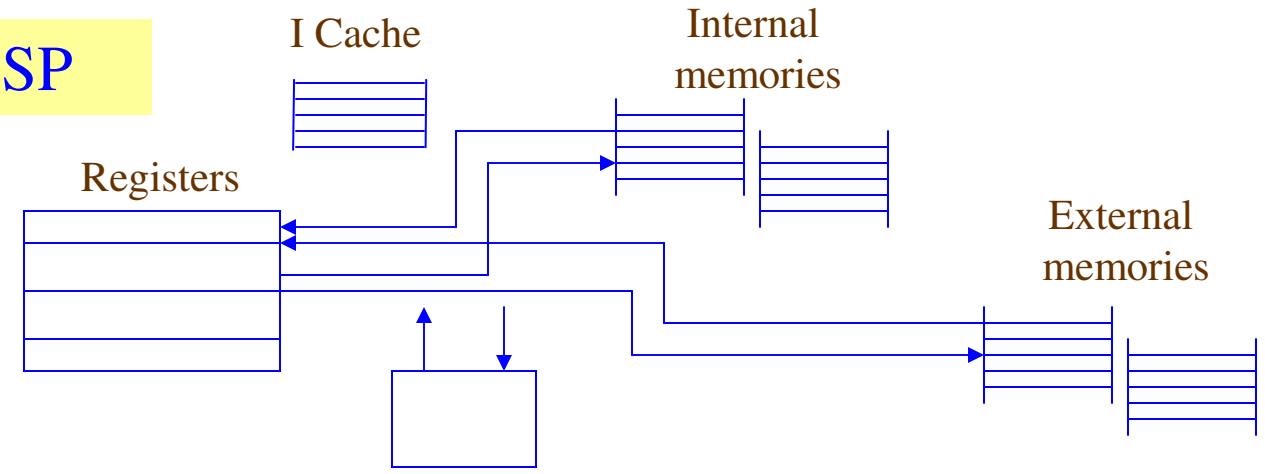
# RISC vs. DSP: Memory Hierarchy

- RISC




*TLB: Translation Lookaside Buffer*

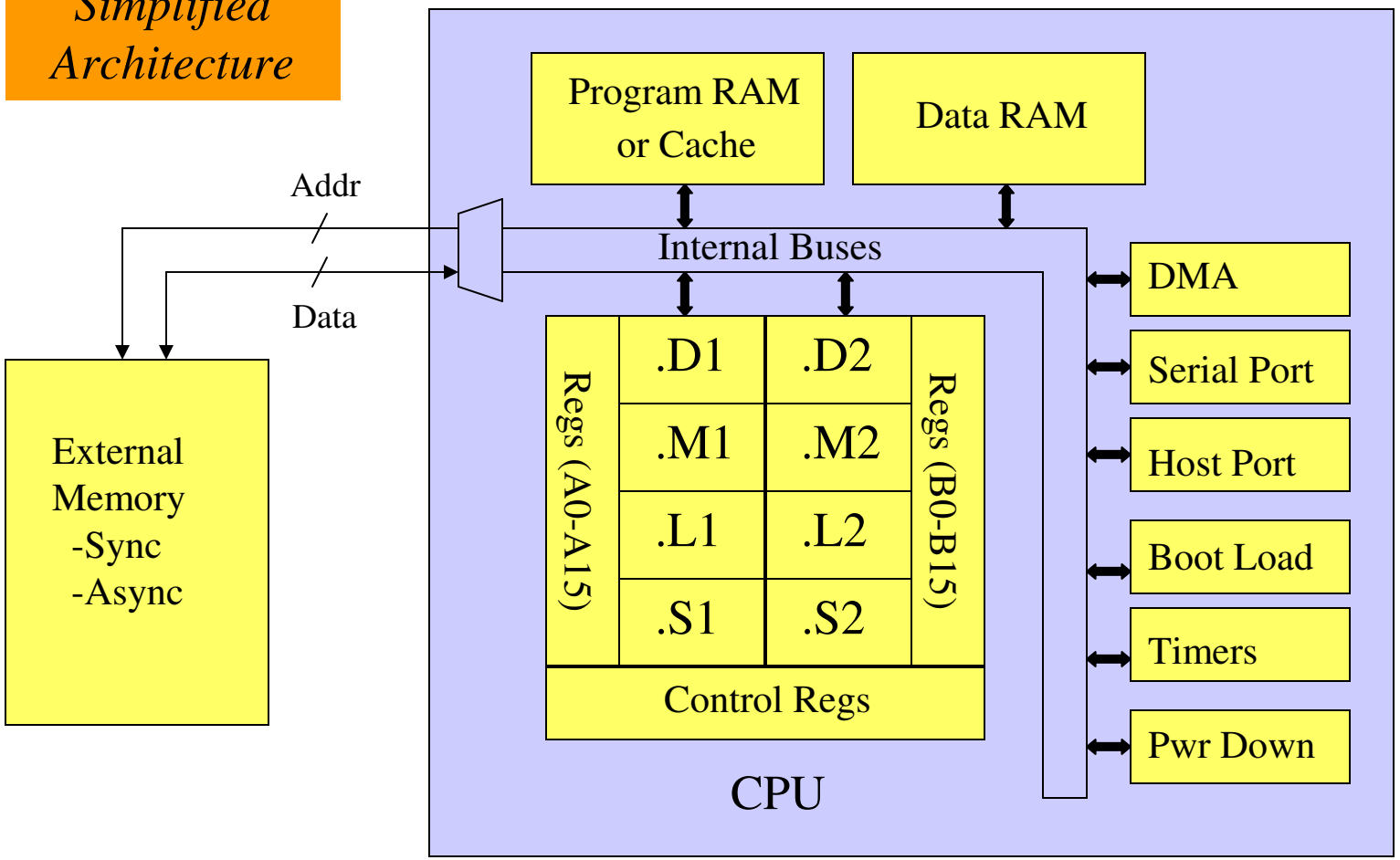
- DSP




*DMA: Direct Memory Access*

# TI TMS320C6000 DSP Architecture

*Simplified Architecture*



# TI TMS320C6000 DSP Architecture

- Very long instruction word (VLIW) size of 256 bits
  - Eight 32-bit functional units with single cycle throughput
  - One instruction cycle per clock cycle
- Data word size is 32 bits
  - 16 (32 on C6400) 32-bit registers in each of 2 data paths
  - 40 bits can be stored in adjacent even/odd registers
- Two parallel data paths
  - Data unit - 32-bit address calculations (modulo, linear)
  - Multiplier unit - 16 bit × 16 bit with 32-bit result
  - Logical unit - 40-bit (saturation) arithmetic & compares
  - Shifter unit - 32-bit integer ALU and 40-bit shifter

# TI TMS320C6000 DSP Architecture

- Families: All support same C6000 instruction set
  - C6200 fixed-pt. 150- 300 MHz ADSL, printers
  - C6400 fixed pt. 300-1,000 MHz video, wireless basestations
  - C6700 floating 100- 300 MHz medical imaging, pro-audio
- TMS320C6701 Evaluation Module (EVM) Board
  - 200 MHz CPU (400 million MACs/s, 1600 RISC MIPS)
  - On-chip memory: 16 kwords program, 16 kwords data
  - On-board: one 133-MHz 64-kword, 2 100-MHz 1-Mword
- TMS320C6713 DSP Starter Kit (DSK) Board
  - 225 MHz CPU (450 million MACs/s, 1800 RISC MIPS)
  - On-chip: 1 kword program, 1 kword data, 16 kword L2
  - On-board memory: 2-Mword SDRAM, 128 kword flash ROM

# TI TMS320C6000 Instruction Set

## C6000 Instruction Set by Functional Unit

| .S Unit | |
|---|---|
| ADD | NEG |
| ADDK | NOT |
| ADD2 | OR |
| AND | SET |
| B | SHL |
| CLR | SHR |
| EXT | SSHL |
| MV | SUB |
| MVC | SUB2 |
| MVK | XOR |
| MVKH | ZERO |

| .L Unit | |
|---|---|
| ABS | NOT |
| ADD | OR |
| AND | SADD |
| CMPEQ | SAT |
| CMPGT | SSUB |
| CMPLT | SUB |
| LMBD | SUBC |
| MV | XOR |
| NEG | ZERO |
| NORM | |

| .D Unit | |
|---|---|
| ADD | ST |
| ADDA | SUB |
| LD | SUBA |
| MV | ZERO |
| NEG | |

| .M Unit | |
|---|---|
| MPY | SMPY |
| MPYH | SMPYH |

| Other | |
|---|---|
| NOP | IDLE |

Six of the eight functional units can perform integer add, subtract, and move operations

# TI TMS320C6000 Instruction Set

***Arithmetic***

ABS
ADD
ADDA
ADDK
ADD2
MPY
MPYH
NEG
SMPY
SMPYH
SADD
SAT
SSUB
SUB
SUBA
SUBC
SUB2
ZERO

***Logical***

AND
CMPEQ
CMPGT
CMPLT
NOT
OR
SHL
SHR
SSHL
XOR

***Bit Management***

CLR
EXT
LMBD
NORM
SET

***Data Management***

LD
MV
MVC
MVK
MVKH
ST

***Program Control***

B
IDLE
NOP

C6000 Instruction Set by Category

(un)signed multiplication
saturation/packed arithmetic

# C6000 vs. C5000 Addressing Modes

- **Immediate**
  - The operand is part of the instruction
- **Register**
  - Operand is specified in a register
- **Direct**
  - Address of operand is part of the instruction (added to imply memory page)
- **Indirect**
  - Address of operand is stored in a register

| *TI C5000* | *TI C6000* |
|---|---|
| `ADD #0FFh` | `add .L1 -13,A1,A6` |
| `(implied)` | `add .L1 A7,A6,A7` |
| `ADD 010h` | `not supported` |
| `ADD *` | `ldw .D1 *A5++[8],A1` |

# TI TMS320C6000 DSP Architecture

**Pentium IV pipeline has more than 20 stages**

- C6000 has deep pipeline
  - 7-11 stages in C6200: fetch 4, decode 2, execute 1-5
  - 7-16 stages in C6700: fetch 4, decode 2, execute 1-10
  - Compiler and assembler must prevent pipeline hazards
- Only branch instruction: delayed unconditional
  - Processor executes next 5 instructions after branch
  - Conditional branch via conditional execution: [A2] B loop
  - Branch instruction in pipeline disables interrupts
  - Undefined if both shifters take branch on same cycle
  - Avoid branches by conditionally executing instructions

*Contributions by Sundararajan Sriram (TI)*

# TI TMS320C6700 Extensions

## C6700 Floating Point Extensions by Unit

***.S Unit***

| | |
|---|---|
| ABSDP | CMPLTSP |
| ABSSP | RCPDP |
| CMPEQDP | RCPSP |
| CMPEQSP | RSARDP |
| CMPGTDP | RSQRSP |
| CMPGTSP | SPDP |
| CMPLTDP | |

***.L Unit***

| | |
|---|---|
| ADDDP | INTSP |
| ADDSP | SPINT |
| DPINT | SPTRUNC |
| DPSP | SUBDP |
| DPTRUNC | SUBSP |
| INTDP | |

***.D Unit***

| | |
|---|---|
| ADDAD | LDDW |

***.M Unit***

| | |
|---|---|
| MPYDP | MPYID |
| MPYI | MPYSP |

Four functional units perform IEEE single-precision (SP) and double-precision (DP) floating-point add, subtract, and move.

Operations beginning with R are reciprocal (i.e. 1/*x*) calculations.

# Selected TMS320C6700 DSPs

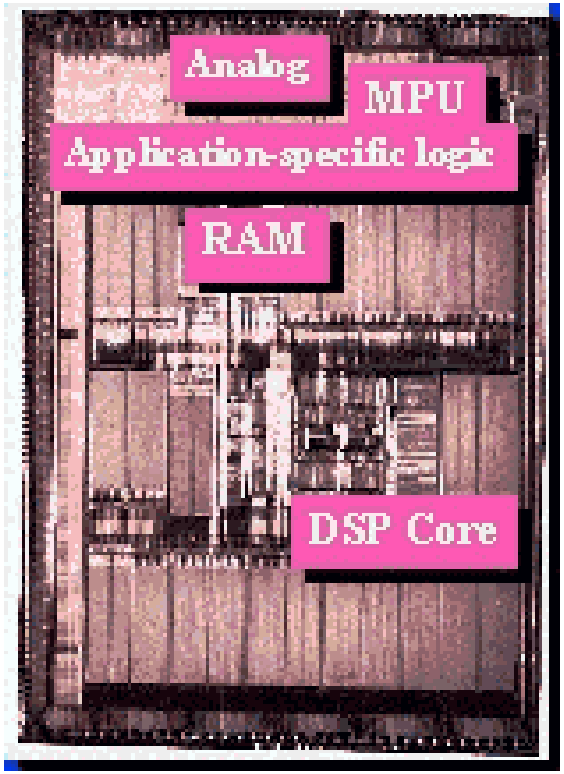
| DSP | MHz | MIPS | Data (kbits) | Program (kbits) | Level 2 (kbits) | Price | Applications |
|---|---|---|---|---|---|---|---|
| C6701 | 150 | 1200 | 512 | 512 | 0 | $ 82 | C6701 EVM board |
| C6711 | 150 | 1200 | 32 | 32 | 512 | $ 22 | C6711 DSK board |
| | 167 | 1336 | | | | $ 20 | |
| | 250 | 2000 | | | | $ 19 | |
| C6712 | 150 | 1200 | 32 | 32 | 512 | $ 14 | |
| C6713 | 167 | 1336 | 32 | 32 | 1000 | $ 21 | |
| | 225 | 1800 | 32 | 32 | 1000 | $ 28 | C6713 DSK board |
| | 300 | 2400 | 32 | 32 | 1000 | $ 39 | |
| C6722 | 250 | 2000 | 1000 | 3072 | 256 | $ 16 | Professional Audio |
| C6726 | 250 | 2000 | 1000 | 3072 | 256 | $ 19 | Professional Audio |

DSK means DSP Starter Kit. EVM means Evaluation Module.

Unit price is for 1,000 units. Prices effective June 3, 2005.

For more information: http://www.ti.com

# Digital Signal Processor Cores




- Application Specific Integrated Circuit (ASIC)
  - Programmable DSP core
  - RAM
  - ROM
  - Standard cells
  - Codec
  - Peripherals
  - Gate array
  - Microcontroller core

# General Purpose Processors

- Multimedia applications on PCs
  - Video, audio, graphics and animation
  - Repetitive parallel sequences of instructions
- Single Instruction Multiple Data (SIMD)
  - One instruction acts on multiple data in parallel
  - Well-suited for graphics
- Native signal processing extensions use SIMD
  - Sun Visual Instruction Set [1995] (UltraSPARC 1/2)
  - Intel MMX [1996] (Pentium I/II/III/IV)
  - Intel Streaming SIMD Extensions (Pentium III)

# DSP on General Purpose Processors (con't)

- Programming is considerably tougher
  - Ability of compilers to generate code for instruction set extensions may lag (e.g. four years for Pentium MMX)
  - Libraries of routines using native signal processing
  - Hand code in assembly for best performance
- Single-instruction multiple-data (SIMD) approach
  - Pack/unpack data not aligned on SIMD word boundaries
  - Saturation arithmetic in MMX; not supported in VIS
  - Extended-precision accumulation in MMX; none in VIS
- Application speedup for Intel MMX and Sun VIS
  - Signal and image processing: 1.5:1 to 2:1
  - Graphics: 4:1 to 6:1 (no packing/unpacking)

# Intel MMX Instruction Set

- 64-bit SIMD register (4 data types)
  - 64-bit quad word
  - Packed byte (8 bytes packed into 64 bits)
  - Packed word (4 16-bit words packed into 64 bits)
  - Packed double word (2 double words packed into 64 bits)
- 57 new instructions
  - Pack and unpack
  - Add, subtract, multiply, and multiply/accumulate
- Saturation and wraparound arithmetic
- Maximum parallelism possible
  - 8:1 for 8-bit additions
  - 4:1 for $8 \times 16$ multiplication or 16-bit additions

# Concluding Remarks

- Conventional digital signal processors
  - High performance vs. power consumption/cost/volume
  - Excel at one-dimensional processing
  - Per cycle: 1 16 × 16 MAC & 4 16-bit RISC instructions
- TMS320C6000 VLIW DSP family
  - High performance vs. cost/volume
  - Excel at multidimensional signal processing
  - Per cycle: 2 16 × 16 MACs & 4 32-bit RISC instructions
- Native signal processing
  - Available on desktop computers
  - Excels at graphics
  - Per cycle: 2 8 × 16 MACs OR 8 8-bit RISC instructions
- Assembly for computational kernels and C for main program (control code, interrupt definition)

# Concluding Remarks

**$9.5B '05 estimated**

- Digital signal processor market
  - 40% annual growth 1990-2000: #1 in semiconductor market
  - Worldwide revenue: $4.4B '99, $6.1B '00, $4.5B '01, $4.9B '02, $6.1B '03, $8.0B '04 (est. annual growth of 23% for 2003-08)
  - 2001: 40% TI, 16% Agere, 12% Freescale, 8% Analog Dev.
  - 2002: 43% TI, 14% Freescale, 14% Agere, 9% Analog Dev.
  - Source: Forward Concepts (http://www.fwdconcepts.com)
- Independent processor benchmarking by industry
  - Berkeley Design Technology Inc. http://www.bdti.com
  - Embedded Microproc. Benchmark Consortium www.eembc.org
- Web resources
  - Newsgroup comp.dsp: FAQ http://www.bdti.com/faq/dsp_faq.html
  - Embedded processors and systems: http://www.eg3.com
  - On-line courses: http://www.techonline.com