Modern Digital Signal Processors

- **Prof. Brian L. Evans**
- **Dept. of Electrical and Computer Engineering**
- **The University of Texas at Austin**

Digital Signal Processor Market

- **Most rapidly expanding sector of semiconductor market (30% growth rate 1990-2001)**
- **600 million cell phone subscribers worldwide (June 2001)**
  - DSPs in more than 60% of existing cell phones
  - 51.7 million cell phone subscribers in 1Q00 in China, the single largest market (30%) in Asia/Pacific (Dataquest)
- ***How many digital signal processors (DSPs) are in each PC? Where are they?***

DSPs on the Market Today

- **Berkeley Design Tech. Inc. Pocket Guide to DSPs**

  http://www.bdti.com/pocket/pocket.htm (see handout)

Big Four Producers of DSPs

	DSP Information / Third-Party Support		Market Share %
Texas Inst.	www.ti.com/sc/docs/dsps/dsphome.htm www.ti.com/sc/docs/dsps/develop/3party.htm	Dallas/ Houston	45
Agere Systems	www.lucent.com/micro/dsp/ no third-party support listed	Allen-town	25
Moto-rola	www.mot.com/SPS/DSP/ www.mot.com/SPS/DSP/developers/thirdparty.html	Austin	10
Analog Devices	www.analog.com/SHARC_2154 www.analog.com/publications/press/products/3rd_party/	Boston/ Austin	8

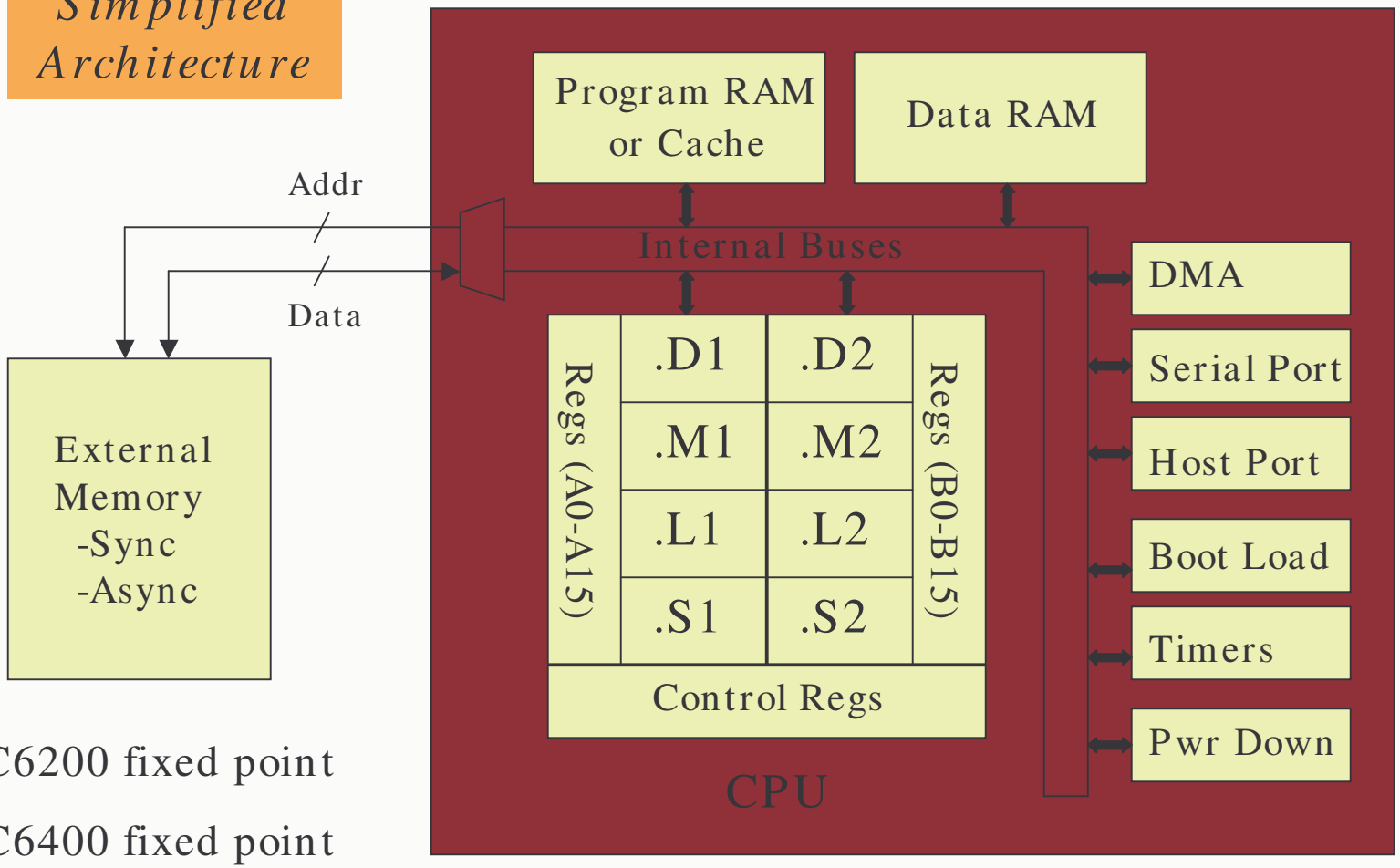
Agere Systems was formerly the Lucent Tech. Microelectronics Group

Texas Instruments

- **First commercially successful DSP**
  - Texas Instruments TMS32010 in 1982
  - Harvey Cragon (UT Austin) was a key part of design team
- **DSP processors shipped**
  - More than 250 million in 1999 (estimated)
- **DSP processor revenue**
  - $2.1 Billion of $4.4 Billion total (48% share) in 1999
  - $2.7 Billion of $6.1 Billion total (44% share) in 2000
- **Modern DSP family is TMS 320C6000**
  - 256-bit instructions: Very Long Instruction Word (VLIW)
  - ADSL modems, 3G basestations, video codecs

C6000 Instruction Set Architecture

Simplified Architecture



C6200 fixed point

C6400 fixed point

C6700 floating point

C6000 Instruction Set Architecture

- **Address 8/16/32 bit data + 64 bit data on C67x**
- **Load-store RISC architecture with 2 data paths**
  - 16 32-bit registers per data path (A0-15 and B0-15)
  - 48 instructions (C62x) and 79 instructions (C67x)
- **Two parallel data paths with 32-bit RISC units**
  - Data unit - 32-bit address calculations (modulo, linear)
  - Multiplier unit - 16 bit x 16 bit with 32-bit result
  - Logical unit - 40-bit (saturation) arithmetic & compares
  - Shifter unit - 32-bit integer ALU and 40-bit shifter
  - Conditionally executed based on registers A1-2 & B0-2
  - Work with two 16-bit halfwords packed into 32 bits

C6000 Functional Units

- **.M multiplication unit**
  - 16 bit x 16 bit signed/unsigned packed/unpacked
- **.L arithmetic logic unit**
  - Comparisons and logic operations (and, or, and xor)
  - Saturation arithmetic and absolute value
- **.S shifter unit**
  - Bit manipulation (set, get, shift, rotate) and branching
  - Addition and packed addition
- **.D data unit**
  - Load/store to memory
  - Addition and pointer arithmetic

C6000 Register Accesses Restrictions

- **Each function unit has read/write ports**
  - Data path 1 (2) units read/write A (B) registers
  - Data path 2 (1) can read one A (B) register per cycle
- **40 bit words stored in adjacent even/odd registers**
  - Used in extended precision accumulation
  - One 40-bit result can be written per cycle
  - A 40-bit read cannot occur in same cycle as 40-bit write
- **Two simultaneous memory accesses cannot use registers of same register file as address pointers**
- **No more than four reads per register per cycle**

C6000 Disadvantages

- **No acceleration for variable length decoding**
  - 50% of computation for MPEG-2 decoding on C6x in C
  - Acceleration available in C6400 family
- **Very deep pipeline**
  - If a branch is in the pipeline, interrupts are disabled: avoid branches by using conditional execution
  - No hardware protection against pipeline hazards: programmer and software tools must guard against it
- **No hardware looping or bit-reversed addressing**
- **40-bit accumulation incurs performance penalty**
- **No status register: must emulate status bits other than saturation bit (.L unit)**

C6700 Floating Point VLIW DSP

- **32-bit floating-point VLIW DSP**
  - Introduced in 1997
  - Extends C6000 instruction set for floating point arithmetic
- **Eight functional units: single cycle throughput**
  - Two ALUs are fixed-point
  - Four ALUs support fixed-point and floating-point
  - Two multipliers support fixed-point and floating-point
- **Applications include professional audio, home entertainment, wireless base stations, medical imaging, sonar imaging, and robotics**

C6712 vs. C6713

- C6712
- 150 MHz clock, 900 MFLOPS
- 4 kB/4kB of L1 program/data memory
- 64 kB of L2 cache
- 1200 MB/s on-chip data bus bandwidth
- $13.50 each in volume

- C6713
- 225 MHz clock, 1350 MFLOPS
- 4 kB/4kB of L1 program/data memory
- 256 kB of L2 cache
- 1800 MB/s on-chip data bus bandwidth
- $26.85 each in volume

Information as of December 3, 2001

TMS320C6200 vs. Pentium

Processor	*Peak MIPS*	*BDTI 2000 marks*	*ISR latency*	*Power*	*Unit Price*	*Area*	*Volume*
Pentium III 1200	2400	2690	1.14 µs	4.25 W	$29	5.5" x 2.5"	8.789 in^3
Pentium III			1.00 µs	4.85 W	n/a	5.5" x 2.5"	8.789 in^3
C6200 200 MHz	1600	1280	0.09 µs	1.94 W	$25	1.3" x 1.3"	0.118 in^3
C6200 300 MHz	2400	1920	0.06 µs		$96	1.3" x 1.3"	0.118 in^3

BDTImarks: Berkeley Design Technology Inc. DSP benchmark results (larger means better) http://www.bdti.com/bdtimark/results.htm

http://www.ece.utexas.edu/~bevans/courses/ee382c/lectures/processors.html

Starcore

- **Startup company with two major investors**
  - Motorola (Semiconductor Product Sector, Austin, TX)
  - Agere Systems (formerly Lucent Technologies Microelectronics Group, Allentown, PA)
- **Has developed 16-bit VLIW DSPs**
  - **SC140**: 300 MHz, 1200 MMACS or 3000 RISC MIPS at 0.2mW/ MMAC at 1.5V or 0.07 mW/MMAC at 0.9V (Jan. 2001 figures)
  - **SC110**: 300 MHz, 300 MMACs or 1200 RISC MIPS, one-half of the peak power consumption of SC140. (Jan. 2001 figures)

TMS320C6200 vs. StarCore S140

Feature	*C6200*	*S140*
Functional Units	8	16
multipliers	2	4
adders	6	4
other	--	8
Instructions/cycle	8	6 + branch
RISC instructions *	8	11
conditionals	8	2
Instruction width (bits)	256	128
Total instructions	48	180
Number of registers	32	51
Register size (bits)	32	40
Accumulation precision (bits) **	32 or 40	40
Pipeline depth (cycle)	7-11	5

* Does not count equivalent RISC operations for modulo addressing

** On the C62x, there is a performance penalty for 40-bit accumulation

Starcore

Lucent StarPro2000	**3 SC140 cores**	**servers and cellular infrastructure**
Motorola MSC8101	**1 SC140 core**	**third-generation wireless systems, IP telephony, modem banks, multi-channel DSL modems**
Motorola MSC8102	**4 SC140 cores**	**high-density multi-channel multi-standard applications, e.g. in central offices of telephone companies and third-generation wireless basestations**

What does Motorola's DigitalDNA slogan mean?

Analog Devices ADSP-21161

- 32-bit floating-point Super Harvard Architecture (SHARC) DSP based on SIMD core (Sept. 6, 2000)
- Single-cycle throughput for fixed-point and floating-point arithmetic
- 100 MHz clock, 600 MFLOPS
- 1 Mbit dual-ported memory
- 800 Mbyte/s of on-chip data bus bandwidth
- $35 each in volumes of 1,000
- Applications include high-end audio systems, wireless basestations, medical imaging, sonar imaging, and robotics

Intel/Analog Devices Blackfin DSP

- **Collaboration begun in Dec. 1999 in Austin, TX**
- **First member ADSP-21535 (June 20, 2001, Webcast)**
- **16-bit fixed-point core**
  - High performance: 1.5V, 300 MHz, 350 mW
  - Low power: 0.9V, 100 MHz, 50 mW
- **2.4 GB on-chip I/O bandwidth at 300 MHz**
- **Dual multiply-accumulate units**
  - 16-bit x 16-bit multiplier
  - 32-bit accumulation
  - 600 million MACs/second at 300 MHz

Intel/Analog Devices Blackfin DSP

- **8 video ALUs**
- **16-bit and 32-bit instructions**
- **Registers**
  - 8 32-bit address registers
  - 8 32-bit data registers
- **Addressability: 8, 16, and 32 bit data**
- **On-core peripherals: PCI, USB, 2 UARTs (one IrDA), A/D and LCD drivers, 3 timers, etc.**
- **Interlocked, eight-stage pipeline**

LSI Logic (Dallas, TX)

- **LSI Logic LSI401Z (Formerly ZSP164xx)**
  - Four-way, in-order superscalar processor
  - 16-bit DSP (16-bit instructions, 16-bit or 32-bit data)

Word size	16-bit instructions and data
	All instructions are 16 bits
Pipeline	5 stages (lock step)
	Fetch 4 instructions
	Issue up to 4 instructions
Branch Prediction	Misprediction rate 30-40% with 5-6 cycle penalty
	Static based on pre-fetch to get offset of target address
Execution	No conditional execution
	2 16-bit ALUs
	2 16x16 multipliers share one 32-bit accumulator

Registers	16 16-bit general-purpose paired as 8 32-bit reg.
	8 reads/instruction
	7 writes/instruction
I/O	DMA (memory mapped reg.)
	Link load
	64-bit input or 32-bit output
	Word alignment
	Not byte addressable
Hardware Addressing	Bit reversed addressing
	2 circular buffers (any length)
	4 nested hardware loops
	64 kw data and 64 kw instr.

Benchmarking

- **Berkeley Design Technology Inc. BDTImark2000**
  - 12 DSP kernels in hand-optimized assembly language
  - Returns single number (higher means faster) per processor
  - Use only on-chip memory (memory bandwidth is the major bottleneck in performance of embedded applications)
- **EDN Embedded Microprocessor Benchmark Consortium (EEMBC pronounced "embassy")**
  - 30 companies formed by Electronic Data News (EDN)
  - Benchmark evaluates compiled C code on a variety of embedded processors (microcontrollers, DSPs, etc.)
  - Application domains: automotive-industrial, consumer, office automation, networking and telecommunications

Battery Technology

- **Key limiting factor in handheld embedded systems**

Battery	*Weight*	*Volume*	*Ratio*
NiCd	55 Wh/kg	145 Wh/l	0.3793 l/kg
NiMH	75 Wh/kg	210 Wh/l	0.3571 l/kg
Li^+	110 Wh/kg	270 Wh/l	0.4074 l/kg
Zn-Air	188 Wh/kg	238 Wh/l	0.7899 l/kg

  - NiMH is Nickel/metal-hydroxide. Used in electric vehicles (see *IEEE Spectrum*, Dec. 1997, p. 69)
  - NiCd, NiMH, and Li+ used in cellular phones
  - Source: Larry Hayes, Motorola Semiconductor Product Sector in Phoenix, Arizona, 1998.