Synchronization with DMT Modulation

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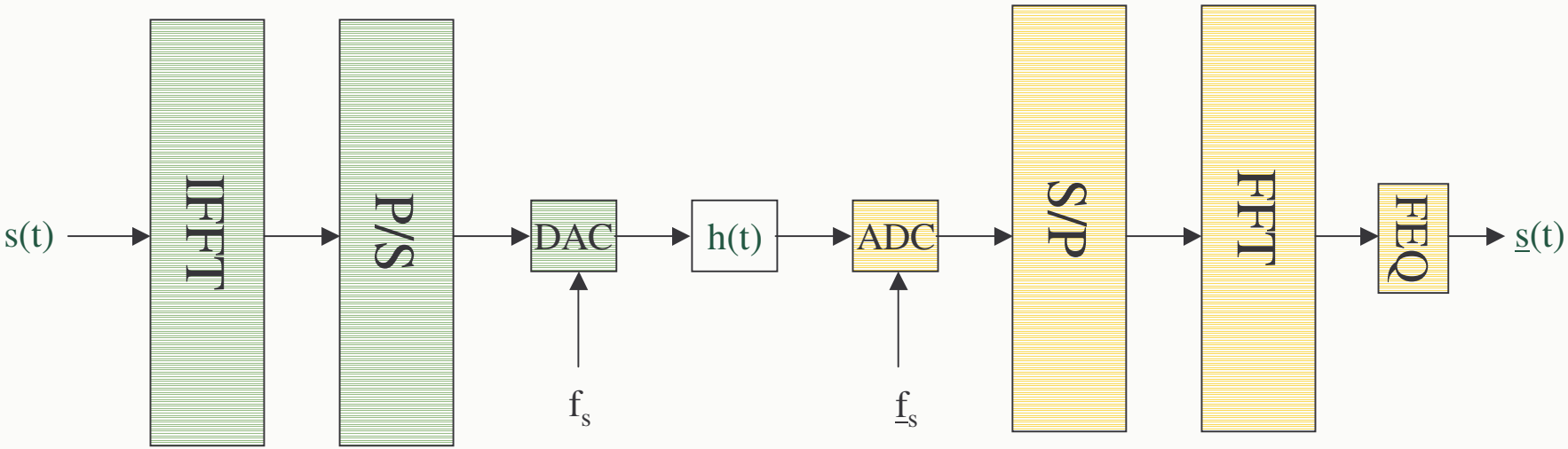
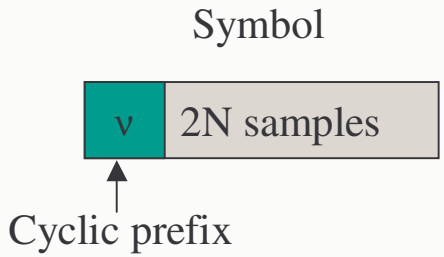
Discrete Multitone Modulation





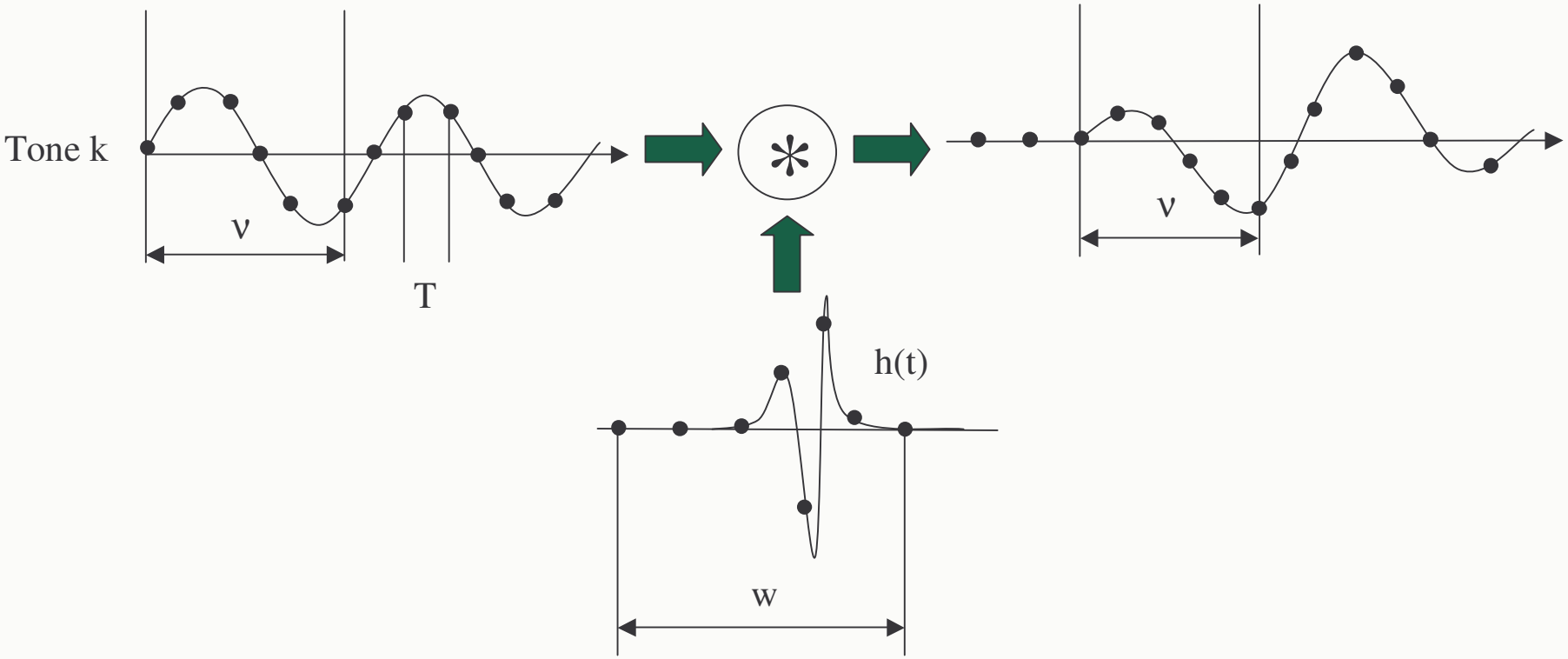
DMT Transceiver

Delay D

Delay D = *integer part* Δ + *fractional part* ε

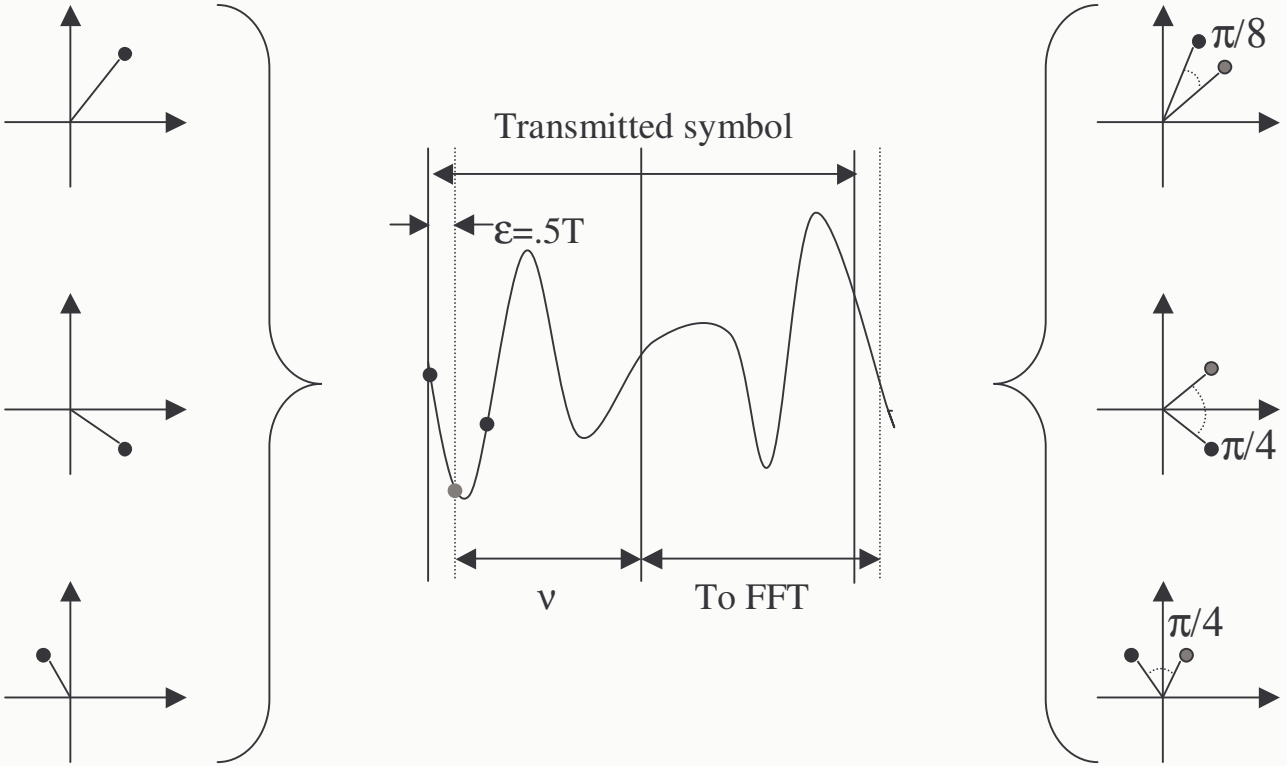
- sample synchronization
  - frequency alignment of RX and TX sampling clocks
  - estimates D
- symbol synchronization
  - insures that proper symbols are fed to the FFT

The Effect of Δ



• ideal synchronizer **delays** RX symbol clock 2 samples w/r to TX symbol clock

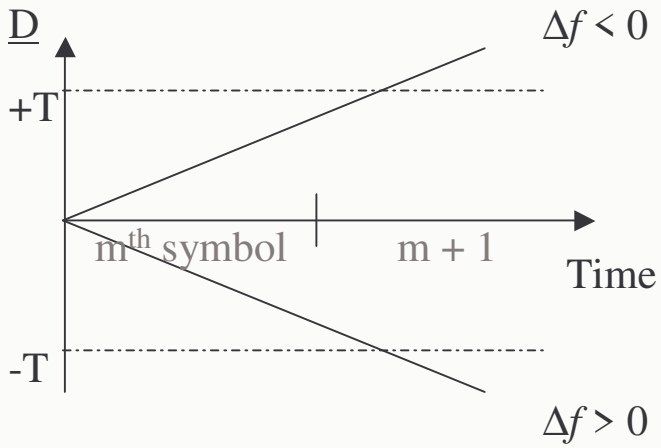
The Effect of ε



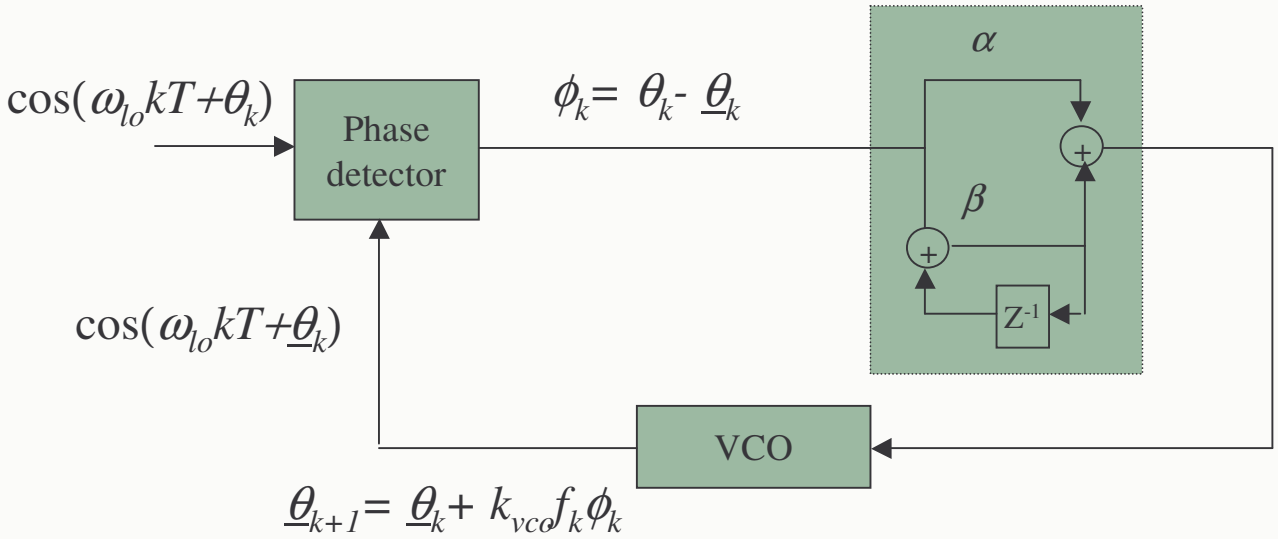
- sample phase shift 0 ⇔ ε ⇔ T => rotation of FFT outputs
- delay-rotor property

The Effect of Frequency Offset

- *RX clock* f_s - *TX clock* f_s $\Delta f \neq 0$ => frequency offset
- timing error increases linearly, intercarrier interference (ICI) is generated
- longer DMT symbols are more sensitive to Δf
- if Δf not minimized the TX and RX clocks will desynchronize



Basic PLL Operation



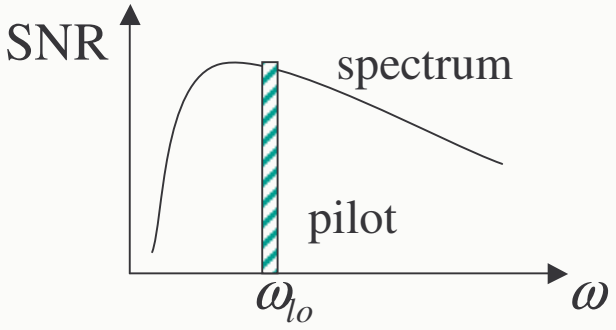
$\Delta f_k = \Delta f_{k+1} + \beta\phi_k$ - frequency offset

$\underline{\theta}_{k+1} = \underline{\theta}_k + \alpha\phi_k + \Delta f_k$ - phase increment

ϕ_k - phase error

Single Pilot Synchronization

- pilot - sinusoid of a known mid-band frequency (ADSL ~ 64KHz)
- bandpass filtering achieved using the FFT
- gives a very accurate PLL reference input signal
- RX modem samples at expected zero-crossings => phase error ϕ_k
- the variance of the timing error can be estimated using



$$\sigma_e^2 << \frac{1}{4\pi^2 f_n^2 \mathrm{SNR}}$$

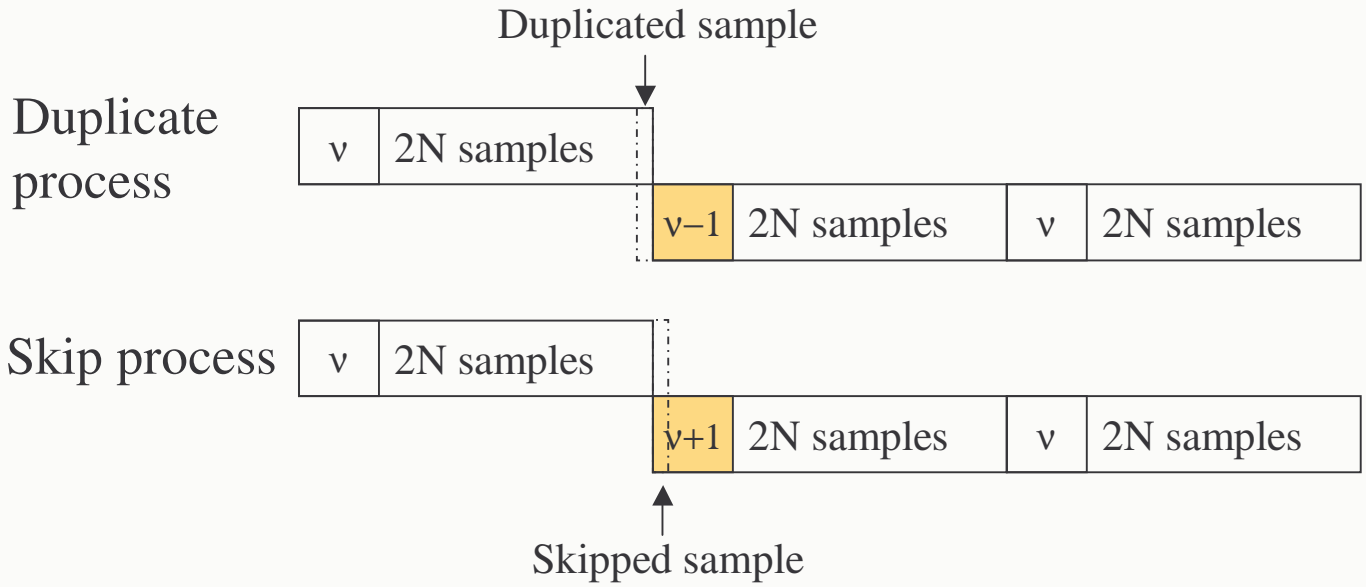
- clock accuracy from 1-2% for ISDN down to 0.1% for ADSL

Phase Offset Correction

- PLL produces a sampling phase offset ϕ
- The signal with timing error $v(t+f) \Rightarrow V(f)\, e^{-j2\pi f\phi}$
- single complex rotation of $(2\pi/n)\phi n$ radians per carrier
- simple, but not correct entirely; $\Delta f \Rightarrow$ all samples have different phase offset (wide-band signal)
- $\phi \sim$ average of all ϕ_n ; more accurate for a shorter symbol

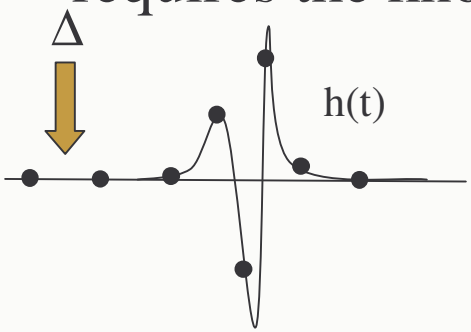
Frequency Offset Correction

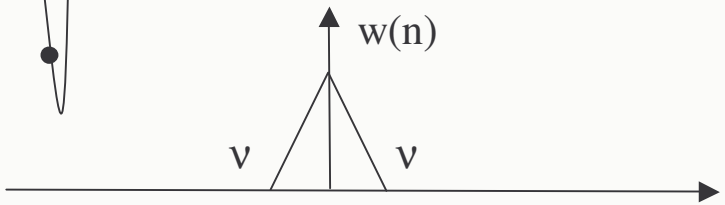
- if $\Delta f \Uparrow$ so that the induced delay $\Leftrightarrow$ to one sample period T a sample is skipped/duplicated in the cyclic prefix
- Δf is adjusted accordingly



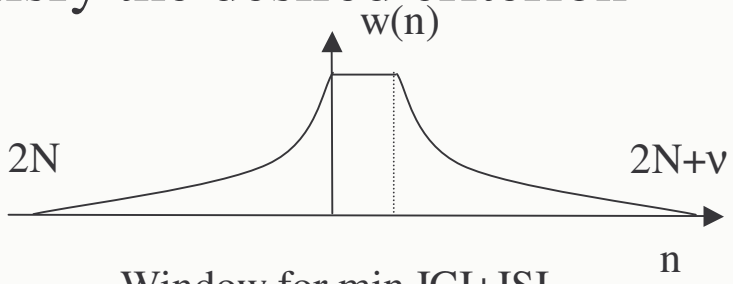
Ad Hoc Symbol Synchronization

- ML criterion not optimal; optimal max. capacity criterion - complex
- try minimizing average ICI + ISI power V(D) ✪ Σ_n $w(n)h^2[(n+D)T]$
- choose a window w(n) that will satisfy the desired criterion
- estimate Δ
- requires the knowledge of h(n)

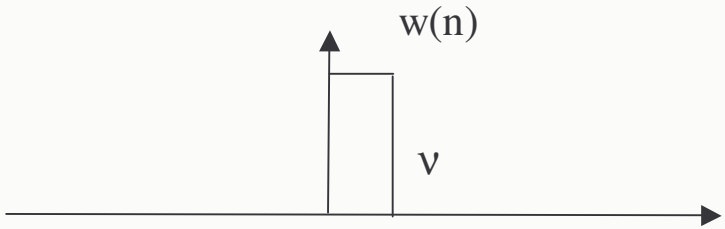




Window for NDA ML estimator

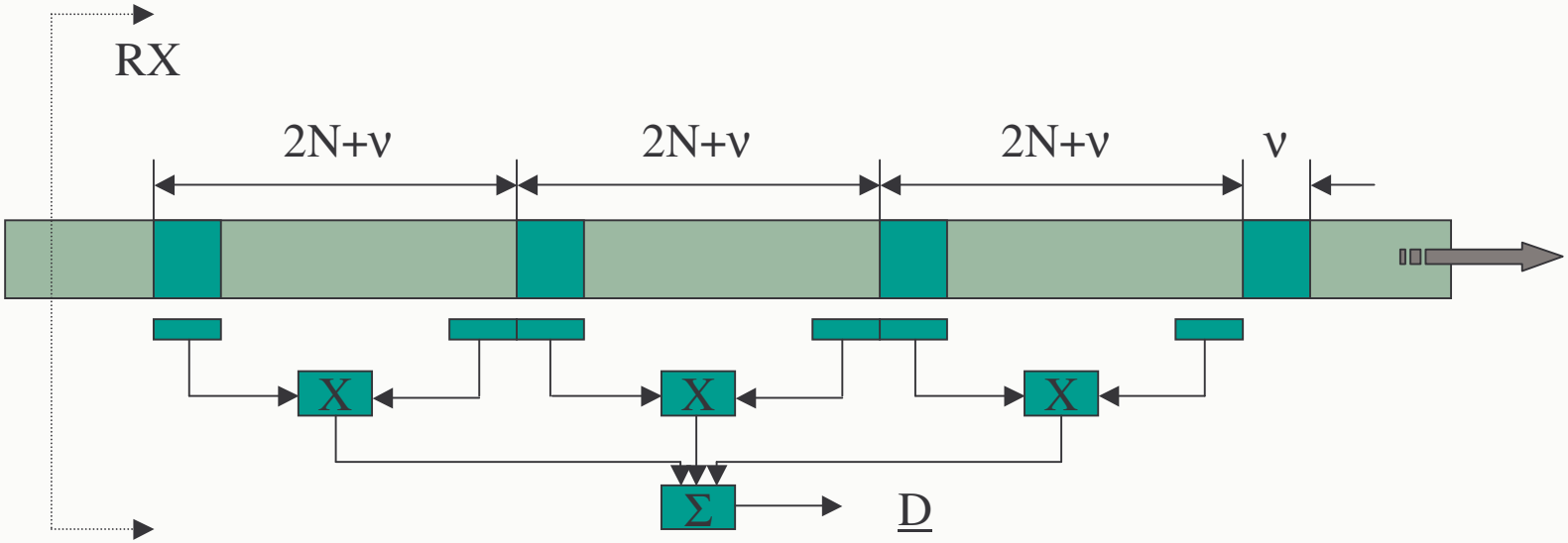


Window for min ICI+ISI



Window for ad-hoc low-complexity estimation

Maximum Likelihood Symbol Synchronization



- maximizing an AWGN likelihood function
- search for Δ that produces the function maximum
- not useful for ε estimation

Sync Symbols

- known symbols embedded in the signal
- used to determine the symbol being transmitted
- in ADSL they occur every 69th frame (T1.413)
- generated by pseudorandom binary signals mapped to 4-bit constellation
- location determined using correlation maximum